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Barbara Villani

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Hon. Commissioner of Patents & Trademarks
Washington, D.C. 20231

Attorney Docket No. 00791/LH

Pursuant to 37 CFR 1.53(b), transmitted herewith for filing is the patent application of

JC825 U.S. PTO
09/704156
11/01/00

Inventor(s): Takeshi WAKABAYASHI

Title: "SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME"

Priority Claim (35 U.S.C. 119) is made, based upon:

Japan No. 11-321416 November 11, 1999

Enclosed herewith are:

[X] Specification (Description, Claims, Abstract): Pages 1 - 21 ; Number of claims 1 - 16

[X] Declaration and Power of Attorney [X] executed; [ ] unexecuted (supplied for information purposes)

[X] 20 Sheets of drawings, Figures 1 - 20 [X] Formal [ ] Informal

[X] Assignment and "Patents" Recordation Form Cover Sheet (PTO-1595) AND $40. RECORDATION FEE.

[X] Certified copy (ies) of priority document(s) identified above

[ ] Information Disclosure Statement; [ ] Form PTO-1449

[ ] Preliminary Amendment

[ ] Verified Statement(s) Claiming Small Entity Status

[X] Receipt Postcard

	Number Filed		Number Extra	Rate	Calculations
Total Claims	16	-20 =	0	x $18.00 =	$
Independent Claims	4	- 3 =	1	x $80.00 =	$ 80.00
MULTIPLE DEPENDENT CLAIMS				+ $270.00 =	$
				BASIC FEE	$ 710.00
				Total of above Calculations	$ 790.00

To the extent not tendered by check, authorization is given to charge any fees under 37 CFR 1.16 and 1.17 during pendency of the application, or to credit any overpayment, to Deposit Account No. 06-1378. Duplicate copy of this letter is enclosed.

FRISHAUF, HOLTZ, GOODMAN, LANGER & CHICK, P.C.

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LH:bv

12/99

TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 11-321416, filed November 11, 1999, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and a method of manufacturing the same. More particularly, the invention relates to a semiconductor device that is sealed in resin in the form of a silicon wafer and a method of manufacturing the same.

A method of manufacturing semiconductor devices called CSPs (Chip Size Packages) will be described with reference to FIG. 17 to FIG. 20. First, as shown in FIG. 17, connection pads 2 are formed on the upper surface of a silicon wafer (semiconductor wafer) 1. An insulating film 3 is then formed, covering the upper surface of the wafer 1 and the connection pads 2, except the center part of each connection pad 2. Wirings 5 are formed, each on a limited region of the insulating film 3 and on the center part of the connection pad 2, which is exposed through an opening 4 made in the insulating film 3. Pillar-shaped

electrodes or column electrodes 6 are formed, each on one end of the wiring 5. Regions 7 shown in FIG. 17 correspond to dicing streets.

Next, as shown in FIG. 18, a seal film 8 made of epoxy-based resin or the like is formed on the upper surface of the resultant structure including the pillar-shaped electrodes 6. The seal film 8 is a little thicker than the pillar-shaped electrodes 6 are tall. The seal film 8 therefore covers the pillar-shaped electrodes 6. Then, the seal film 8 is polished at its upper surface until the tops of the pillar-shaped electrodes 6 are exposed as is shown in FIG. 19. Further, the silicon wafer 1 is cut along the dicing streets 7. Chips, or semiconductor devices 9, are thereby manufactured as is illustrated in FIG. 20.

The semiconductor devices 9 have been made by cutting the silicon wafer 1 that has the seal film 8 formed on it along the dicing streets 7. The four sides of each semiconductor device 9 are therefore exposed. At the exposed sides, water or moisture may enter the interface between the insulating film 3 (protective film) and the seal film 8, and may oxidize the wirings 5 and the like. Moreover, a crack or cracks may develop in the interface between the insulation film 3 and the seal film 8.

BRIEF SUMMARY OF THE INVENTION

An object of the present invention is to provide

a semiconductor device that is resin-sealed at the sides, too, which are exposed when the device is cut from a wafer.

According to an aspect of the invention there is provided a semiconductor device which comprises a semiconductor substrate and a seal film. The substrate has an upper surface, a lower surface opposing the upper surface, sides extending between the upper and lower surfaces, and a plurality of outer connection terminals formed on the upper surface. The seal film covers the upper surface of the semiconductor substrate, exposes each of the outer connection terminals at one surface, and covers the sides to at least half the thickness of the semiconductor substrate.

According to another aspect of invention there is provided a method of manufacturing a semiconductor device. The method comprises the steps of: preparing a semiconductor wafer having an upper surface, a lower surface opposing the upper surface, sides extending between the upper and lower surfaces, and a plurality of outer connection terminals formed on the upper surface; making trenches in those parts of the semiconductor wafer which lie between chip-forming regions thereof, each trench reaching at least half the thickness of the semiconductor wafer, and forming a seal film on the upper surface of the semiconductor

wafer, filling the trenches and exposing the outer connection terminals at one surface; and cutting the seal film along the trenches, removing those parts of the seal film which have a smaller width than the trenches.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out hereinafter.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the invention, and together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

FIG. 1 is a magnified, sectional view of a silicon wafer having pillar-shaped electrodes on it, for explaining a step of a method of manufacturing a semiconductor device according to the first embodiment of the invention;

FIG. 2 is also a magnified, sectional view of the silicon wafer, explaining the step that follows the

step shown in FIG. 1;

FIG. 3 is a magnified, sectional view of the silicon wafer, explaining the step that follows the step shown in FIG. 2;

FIG. 4 is magnified, sectional view of the silicon wafer, explaining the step that follows the step shown in FIG. 3;

FIG. 5 is magnified, sectional view of the silicon wafer, explaining the step that follows the step shown in FIG. 4;

FIG. 6 is magnified, sectional view of the silicon wafer, explaining the step that follows the step shown in FIG. 5;

FIG. 7 is magnified, sectional view of the silicon wafer, explaining the step that follows the step shown in FIG. 6;

FIG. 8 is magnified, sectional view of the silicon wafer, explaining the step that follows the step shown in FIG. 7;

FIG. 9 is magnified, sectional view of the silicon wafer, explaining the step that follows the step shown in FIG. 8;

FIG. 10 is magnified, sectional view of the silicon wafer, explaining the step that follows the step shown in FIG. 9;

FIG. 11 is a magnified, sectional view of a silicon wafer, explaining a step of a method of

manufacturing a semiconductor device that is the second embodiment of this invention;

FIG. 12 is a magnified, sectional view of the silicon wafer, explaining the step that follows the step shown in FIG. 11;

FIG. 13 is a magnified, sectional view of a silicon wafer, explaining a step of a method of manufacturing a semiconductor device that is the third embodiment of this invention;

FIG. 14 is a magnified, sectional view of a silicon wafer, explaining a step of a method of manufacturing a semiconductor device that is the fourth embodiment of the invention;

FIG. 15 is a magnified, sectional view of the silicon wafer, explaining the step that follows the step explained in FIG. 14;

FIG. 16 is a magnified, sectional view of a silicon wafer, explaining a step of a method of manufacturing a semiconductor device that is the fifth embodiment of the invention;

FIG. 17 is a magnified, sectional view of a silicon wafer, explaining a conventional method of manufacturing a semiconductor device;

FIG. 18 is a magnified, sectional view of the silicon wafer, explaining the step that follows the step shown in FIG. 17;

FIG. 19 is a magnified, sectional view of the

silicon wafer, explaining the step that follows the step shown in FIG. 18; and

FIG. 20 is a magnified, sectional view of the silicon wafer, explaining the step that follows the step shown in FIG. 19.

DETAILED DESCRIPTION OF THE INVENTION

FIGS. 1 to 10 show the steps of manufacturing a semiconductor device according to the first embodiment of the present invention. With reference to the figures, the structure of the semiconductor device will be described, along with the method of manufacturing the semiconductor device. First, an unfinished product is prepared. As shown in FIG. 1, the unfinished product comprises a silicon wafer (semiconductor wafer) 1 and pillar-shaped electrodes (outer connection terminals) 6 formed on the upper surface thereof. Integrated circuits are provided in the inner area on the silicon wafer 1. More specifically, the unfinished product is prepared as follows. First, connection pads 2 are formed on the upper surface of the silicon wafer 1 and are connected to the integrated circuits provided on the silicon wafer 1. An insulating film 3 is then formed, covering the upper surface of the wafer 1 and the connection pads 2, except the center part of each connection pad 2. The insulating film 3 is formed of a single layer made of silicon oxide, silicon nitride, or the like. Alternatively, the film 3 may be a

multi-layer film comprising a silicon oxide film, a silicon nitride film or the like and an organic protective film made of polyimide or the like. Wirings 5 are then formed, each on a limited region of the insulating film 3 and on the center part of the connection pad 2, which is exposed through an opening 4 made in the insulating film 3. Finally, pillar-shaped electrodes 6 (outer connection terminals) are formed, each on one end of the wiring 5. Regions 7 shown in FIG. 1 correspond to dicing streets in a shape of matrix.

Next, as shown in FIG. 2, a dicing tape 11 is adhered to the lower surface of the silicon wafer 1. The dicing tape 11 is firmly adhered to the silicon wafer 1 because its upper surface is coated with adhesive. As shown in FIG. 3, the silicon wafer 1 is cut along the dicing streets 7. In order to cut the wafer 1 completely, through its thickness, the dicing tape 11 is cut, too, in part or to half its thickness. The silicon wafer 1 is thereby cut into semiconductor substrates 1', each being a semiconductor chip. Nonetheless, the substrates 1' will be collectively called "silicon wafer 1," since the dicing tape 11 is adhered to the lower surfaces of the substrates 1', fastening the semiconductor substrates 1' together. Once the silicon wafer 1 is completely cut and the dicing tape 11 is cut in part, trenches 12 having

a prescribed width are formed among the semiconductor substrates 1'.

Thereafter, as shown in FIG. 4, a seal film 13 made of epoxy-based resin or the like is formed on the upper surface of the silicon wafer 1 having the pillar-shaped electrodes 6 and the trenches 12. The seal film 13 is a little thicker than the pillar-shaped electrodes 6 are tall. The seal film 13 therefore covers the pillar-shaped electrodes 6 and filling the trenches 12. In this condition, the seal film 13 completely covers the four sides 1a of each semiconductor substrate 1'. Then, the seal film 13 is polished at its upper surface until the tops of the pillar-shaped electrodes 6 are exposed as is shown in FIG. 5. Thereafter, the pillar-shaped electrodes 6 may be surface-treated, to form an oxidation-preventing layer on the top surface of the electrode 6.

Next, as shown in FIG. 6, the seal film 13 is cut into segments, along the trenches 12, more precisely, substantially along the centerlines of the trenches 12. Now that the seal film 13 is thus cut, the semiconductor substrates 1' (or chips) can be separated from one another if the dicing tape 11 is completely cut. In this condition, too, the four sides 1a of each semiconductor substrate 1' remain covered with the seal film 13 provided in the trenches 12. Further, as shown in FIG. 7, a support tape 14 is adhered to the tops

of segments of the seal film 13 and the tops of the pillar-shaped electrodes 6. Then, the dicing tape 11 is peeled off, whereby the structure shown in FIG. 8 is obtained. As shown in FIG. 8, each seal film segment 13 has parts 13a extending through the trenches 12 and projecting from the lower surface of the silicon wafer 1. Since the support tape 14 is adhered to the tops of the seal film segments and the tops of the pillar-shaped electrodes 6, the semiconductor substrates 1' (or chips) remain combined together.

Then, the parts of the segments of the seal film 13, which project from the lower surface of the wafer 1 are polished and removed. The structure shown in FIG. 9 is thereby provided. Thereafter, the lower surface of the silicon wafer 1 may be polished. Finally, the support tape 14 is peeled off. As a result, semiconductor devices 15, or semiconductor chips, are manufactured as is illustrated in FIG. 10.

In each of the semiconductor devices 15 thus manufactured, the seal film (segment) 13 covers the four sides 1a of the semiconductor substrate 1'. This prevents water or moisture from entering the interface between the insulating film 3 (protective film) and the seal film 13 and may oxidize the wirings 5 and the like. Moreover, a crack hardly develops in the interface between the insulation film 3 and the seal film 13.

FIG. 11 and FIG. 12 are cross sectional views explaining a method of manufacturing a semiconductor device according to the second embodiment of the invention. In this method, a silicon wafer 1 is cut at its upper surface, but only to half its thickness, along dicing streets 7, as is illustrated in FIG. 11. In other words, U-trenches 12 are made in the upper surface of the silicon wafer 1, at those regions of the wafer 1 which correspond to dicing streets 7. Thereafter, a seal film 13 is formed in the same way as in the first embodiment. Then, as shown in FIG. 12, the seal film 13 and the silicon wafer 1 are cut along the dicing streets 7, thereby providing semiconductor devices 15 (or semiconductor chips). In the second embodiment, the four sides 1a of each semiconductor substrate 1' are covered with the seal film 13, from the upper edge of the substrate 1' to half the thickness of the substrate 1'.

In the semiconductor device 15 made by the first embodiment, each side 1a of the semiconductor substrate 1' is a vertical surface, which is entirely covered with the seal film 13 as is illustrated in FIG. 10. In the semiconductor device made by the second embodiment, each side 1a of the semiconductor substrate 1' comprises a lower vertical surface, an upper vertical surface and a horizontal surface extending between the vertical surfaces and positioned under the

interface between the films 3, 13, as is illustrated in FIG. 12. Of these three surfaces, the upper vertical surface and the horizontal surface are covered with the seal film 13. Hence, water or moisture is prevented from entering the interface between the insulating film 3 and the seal film 13, and a crack hardly develop in the interface between the insulation film 3 and the seal film 13, as in the semiconductor device manufactured by the first embodiment.

FIG. 13 is a sectional view explaining a method of manufacturing a semiconductor device according to the third embodiment of the invention. As in the first embodiment, each side 1a of the semiconductor substrate 1' is a vertical surface, which is entirely covered with the seal film 13. In the third embodiment, however, the semiconductor substrate 1' is thinner than in the first embodiment. The semiconductor devices 15 shown in FIG. 13 can be made by the method of the second embodiment. More precisely, U-trenches 12 are made in the upper surface of the silicon wafer 1 as shown in FIG. 11, and a seal film 13 is then formed and filling the U-trenches 12 but not covering the pillar-shaped electrodes 6, as is illustrated in FIG. 12. Then, the silicon wafer 1 is polished, at its lower surface, to the bottoms of the U-trenches. Semiconductor substrates 1' are thereby provided. Each semiconductor substrate 1' thus provided has its four

sides 1a covered with the seal film 13. Thereafter, the seal film 13 is cut along the U-trenches 12 of the substrate 1'. As a result, semiconductor devices 15 are obtained, as is illustrated in FIG. 13.

FIG. 14 and FIG. 15 are sectional views explaining a step of a method of manufacturing a semiconductor device according to the fourth embodiment of the present invention. In this method, a seal film 17 made of epoxy-based resin or the like is formed on the lower surface of a silicon wafer 1 as is shown in FIG. 14. A peel layer 16 is formed on the lower surface of the seal film 17. Further, a dicing tape 11 is adhered to lower surface of the peel layer 16. Then, the silicon wafer 1 is cut along dicing streets 7, to half the thickness of the seal film 17 or to the lower surface of the seal film 17. Semiconductor substrates 1', or semiconductor chips, are thereby obtained as is shown in FIG. 15. Thereafter, a seal film 13 is formed on the silicon wafer 1, filling the gaps between the semiconductor substrates 1'. As a result, the upper surface, lower surface and four sides 1a of each semiconductor substrate 1' are covered with the seal films 13 and 17, as is illustrated in FIG. 15. Then, the seal film 13 is cut, removing those parts corresponding to the dicing streets 7 and having a smaller width than the gaps the semiconductor substrates 1'. Semiconductor devices 15 are thereby

made as is shown in FIG. 15. In the fourth embodiment, each semiconductor substrate 1' is covered not only at the upper surface and four sides 1a, but also at the lower surface with integrated films 13, 17. The seal film 17 is cut, together with the seal film 13. Since the lower surface of the substrate 1' is covered with the seal film 17, the substrate 1' is protected from light and electromagnetic waves applied to the lower surface of the silicon substrate 1'. In the fourth embodiment, the silicon wafer 1 may be polished at its lower surface, in order to reduce the thickness of the semiconductor devices 15.

FIG. 16 is a sectional view explaining a method of manufacturing a semiconductor device according to the fifth embodiment of the invention.

In the fifth embodiment, a seal film 17 is formed on the lower surface of a silicon wafer 1. Then, U-trenches 12 are made in the upper surface of the silicon wafer 1, by cutting the wafer 1 from the upper surface to half the thickness of the wafer 1. A seal film 13 is formed on the upper surface of the silicon wafer 1 such that the tops of pillar-shaped electrodes 6 remain exposed. At this time, the seal film 13 fills the U-trenches in the wafer. Thereafter, the seal film 13, silicon wafer 1 and seal film 17 are integrally cut, thus removing those parts corresponding to the dicing streets 7 and having a smaller width than

that of the U-trench. Semiconductor devices 15 are thereby made. In the fifth embodiment, it is desired that a dicing tape (not shown in FIG. 16) be kept adhered to the seal film 17 until the silicon wafer 1 are cut to provide semiconductor devices 15.

In any embodiment described above, a seal film is formed on a silicon wafer 1 that has connection pads 2, wirings 5 connected to the pads 2 and pillar-shaped electrodes 6 provided on the wirings 5. Instead, no wirings 5 may be formed, and the seating film may be formed on the assembly including the pillar-shaped electrodes 6 formed directly on the connection pads 2. Moreover, the pillar-shaped electrodes 6 may be outer connection terminals, which are connected to the connection pads 2 by means of wire bonding. If this is the case, it suffices to make openings in the seal film, thus exposing the connection pads 2.

As has been described above, the side of each silicon substrate is covered with a seal film, at least at their upper part, in the present invention. Thus, at least the upper part of the side is never exposed. This reliably protects the side of each silicon substrate.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments

shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate having an upper surface, a lower surface opposing the upper surface, sides extending between the upper and lower surfaces, and a plurality of outer connection terminals formed on the upper surface; and

a seal film covering the upper surface of the semiconductor substrate, exposing the outer connection terminals at one surface, and covering the sides, to at least half the thickness of the semiconductor substrate.

2. The semiconductor device according to claim 1, wherein the seal film covering the upper surface of the semiconductor substrate is substantially flush with the upper surfaces of the outer connection terminals.

3. The semiconductor device according to claim 1, wherein the seal film covers the sides in entirety.

4. The semiconductor device according to claim 1, wherein the seal film covers the sides to half the thickness of the semiconductor substrate.

5. The semiconductor device according to claim 4, wherein the faces of the seal film that covers the sides of the semiconductor substrate are substantially flush with the sides of that part of the semiconductor substrate which are not covered with the seal film.

6. The semiconductor device according to claim 1,

wherein the seal film cover all surfaces and sides of the semiconductor substrate.

7. A semiconductor device comprising:

a semiconductor substrate having an upper surface and sides;

a plurality of connection pads formed on one surface of the semiconductor substrate;

an insulating film having openings exposing the connection pads and covering said upper surface of the semiconductor substrate;

wiring connected to the connection pads and provided on the insulating film;

pillar-shaped electrodes connected to the wirings and having top surfaces; and

a seal film exposing the pillar-shaped electrodes at the top surface and covering the upper surface of the semiconductor substrate and portions of the sides extending to at least half the thickness of the semiconductor substrate from the top surface.

8. The semiconductor device according to claim 7, wherein the seal film covering the upper surface of the semiconductor substrate is substantially flush with the top surfaces of the pillar-shaped electrodes.

9. The semiconductor device according to claim 7, wherein the seal film covers the sides of the semiconductor substrate in entirety.

10. The semiconductor device according to claim 7,

wherein the seal film covers all surfaces and sides of the semiconductor substrate.

11. A method of manufacturing a semiconductor device comprising the steps of:

preparing a semiconductor wafer having an upper surface, a lower surface opposing the upper surface, sides extending between the upper and lower surfaces, and a plurality of outer connection terminals formed on the upper surface;

making trenches in those parts of the semiconductor wafer which lie between chip-forming regions thereof, each trench extending at least half the thickness of the semiconductor wafer from the upper surface;

forming a seal film on the upper surface of the semiconductor wafer, filling the trenches and exposing the outer connection terminal at one surface; and

cutting the seal film along the trenches, removing those parts of the seal film which have a smaller width than the trenches.

12. The method according to claim 11, further comprising a step of adhering a dicing tape to the semiconductor wafer before the trenches are made in the semiconductor wafer.

13. The method according to claim 12, further comprising a step of adhering a support tape to an upper surface of the seal film after the seal film

is cut, and a step of peeling the dicing tape from the semiconductor wafer.

14. The method according to claim 11, further comprising a step of polishing a lower surface of the semiconductor wafer after the seal film is cut, thereby reducing the thickness of the semiconductor wafer.

15. The method according to claim 11, another seal film is formed on a lower surface of the semiconductor wafer before the seal film is cut.

16. A method of manufacturing a semiconductor device, comprising the steps of:

preparing a semiconductor wafer having an upper surface and sides and having a plurality of connection pads on the upper surface;

forming an insulating film having openings exposing the connection pads, thereby covering the upper surface of the semiconductor wafer;

forming wirings on the insulating film, said wirings connected to the connection pads;

forming pillar-shaped electrodes on the wirings; and

forming a seal film exposing the pillar-shaped electrodes at one surface and covering the upper surface of the semiconductor wafer and the part of the sides extending to at least half the thickness of the semiconductor wafer from the upper surface.

ABSTRACT OF THE DISCLOSURE

A dicing tape is adhered to the lower surface of a silicon wafer that has pillar-shaped electrodes. The silicon wafer is cut along dicing streets, thereby making trenches among the chip-forming regions of the wafer. Next, a seal film is formed. The seal film is cut, substantially along the centerlines of the trenches. A support tape is adhered to the upper surface of the seal film. The dicing tape is peeled off. Then, those parts of the seal film that project from the lower surface of the silicon wafer are polished and removed. The support tape is peeled off. IC chips are thereby obtained. In each IC chip, the seal film covers and protects the upper surface and sides of the semiconductor substrate.

FIG.1

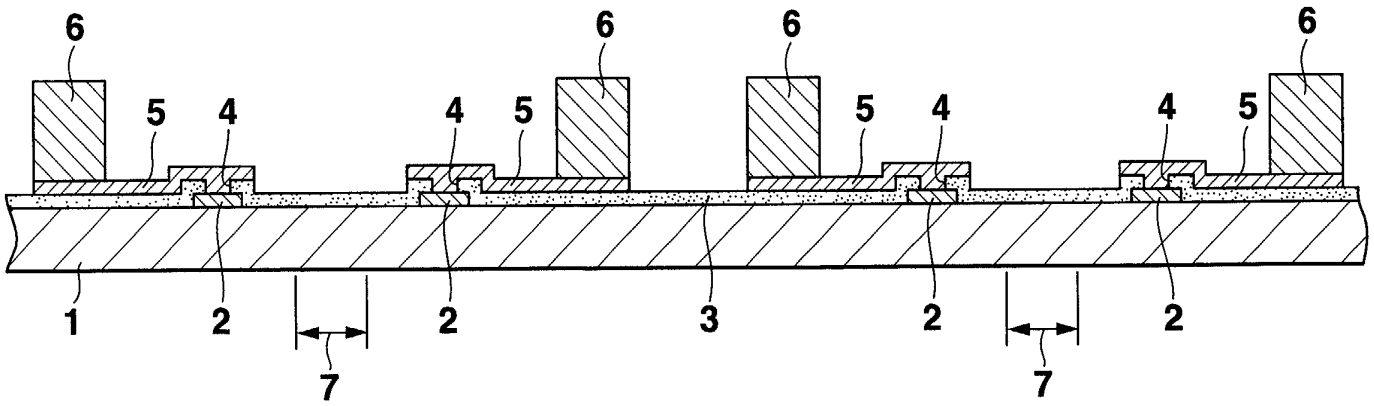


FIG.2

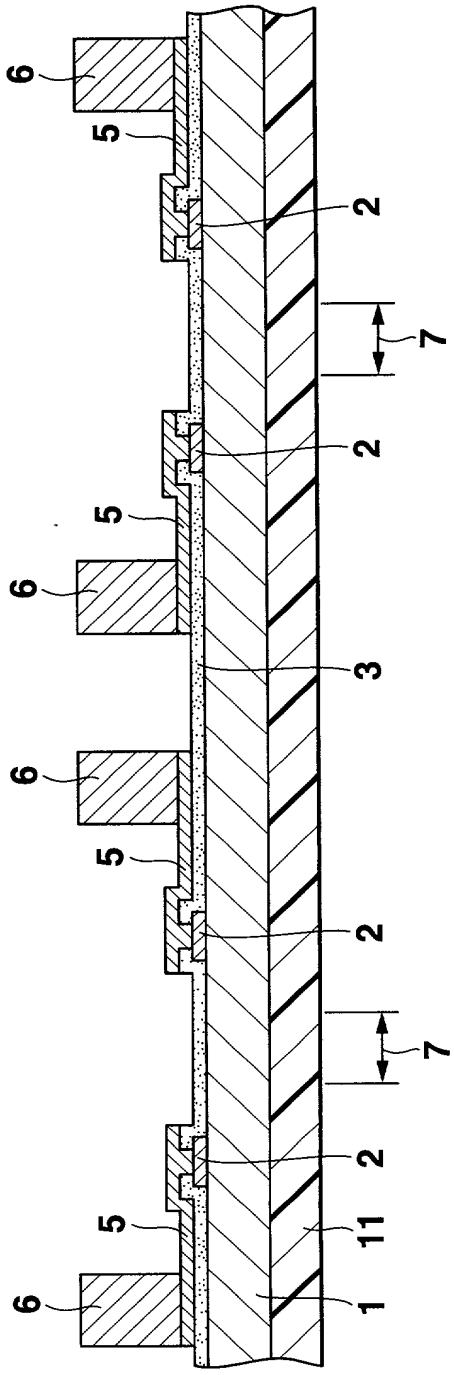


FIG.3

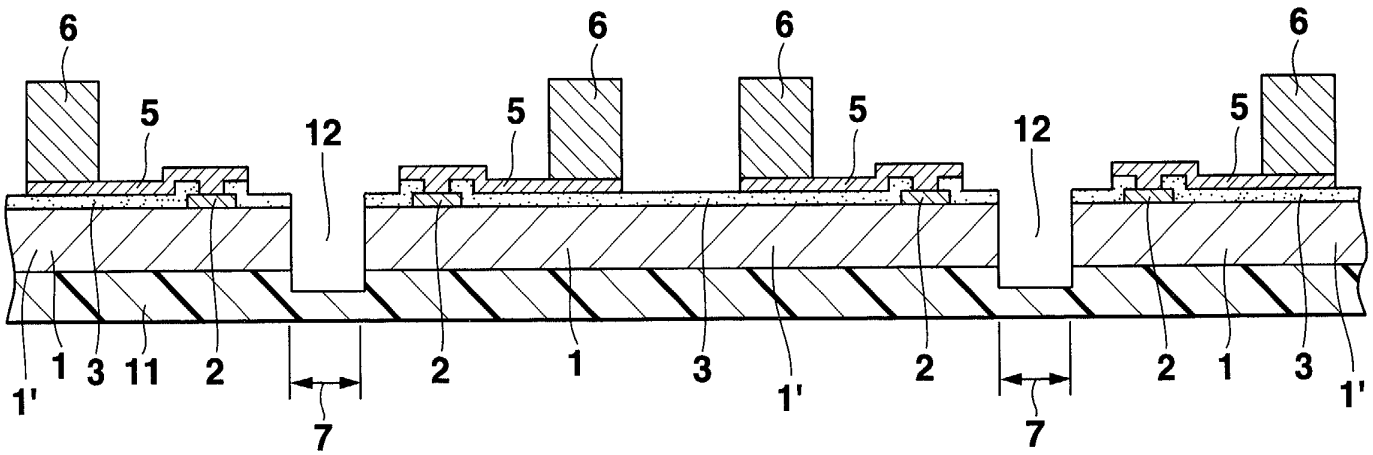


FIG.4

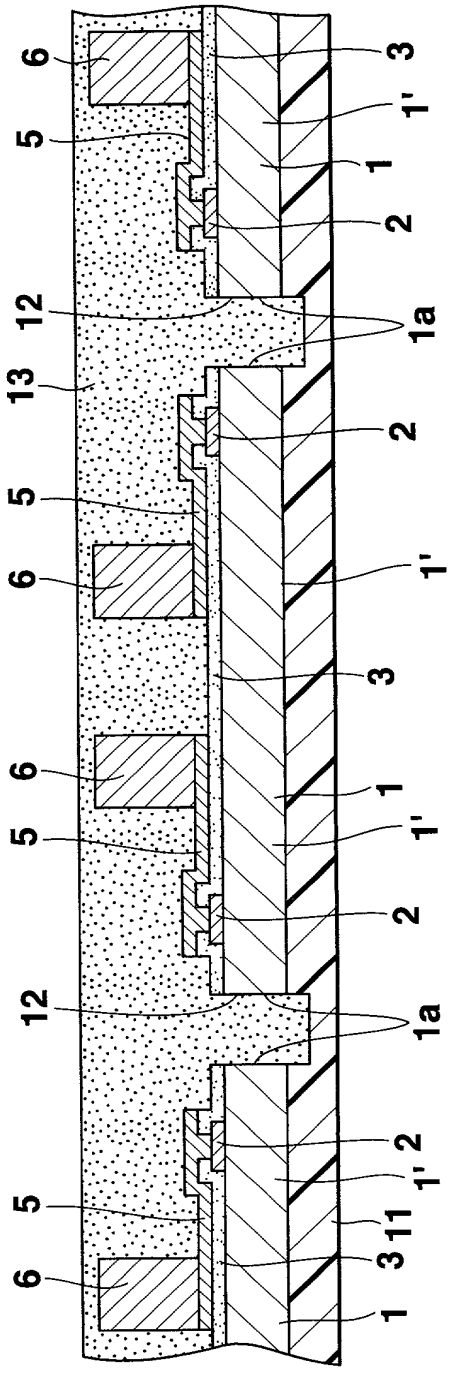


FIG.5

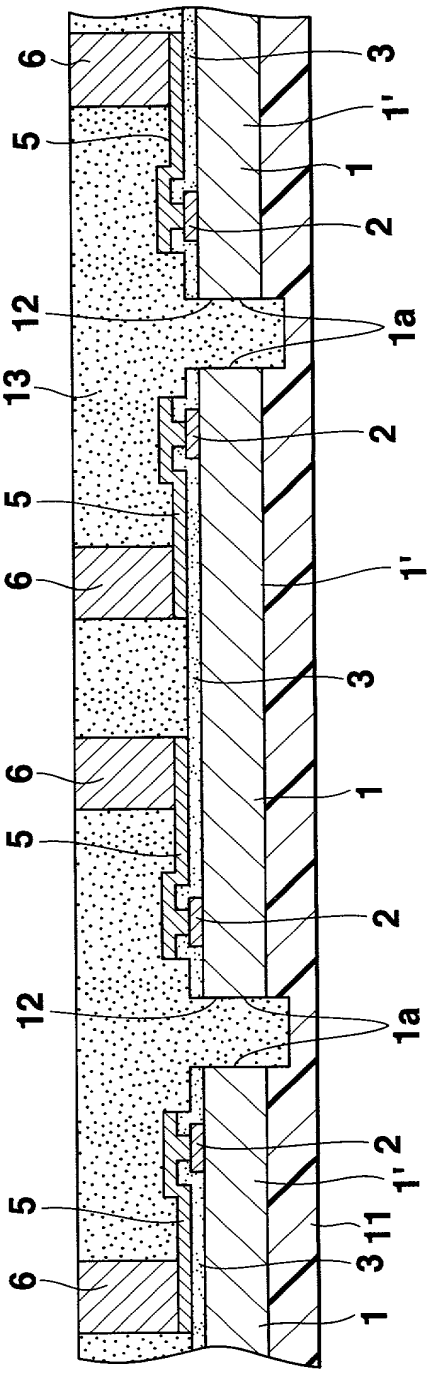


FIG.6

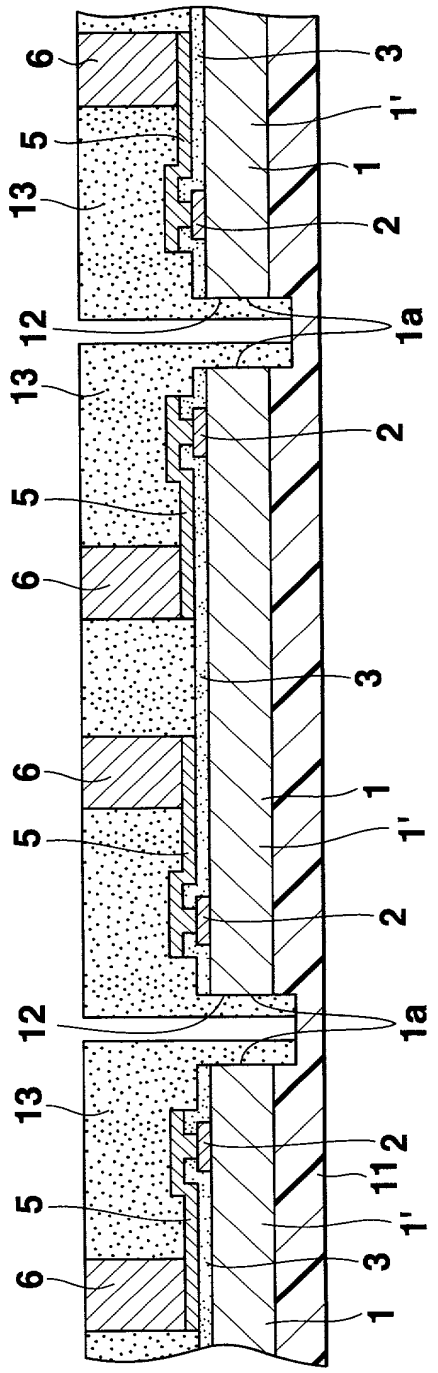


FIG.7

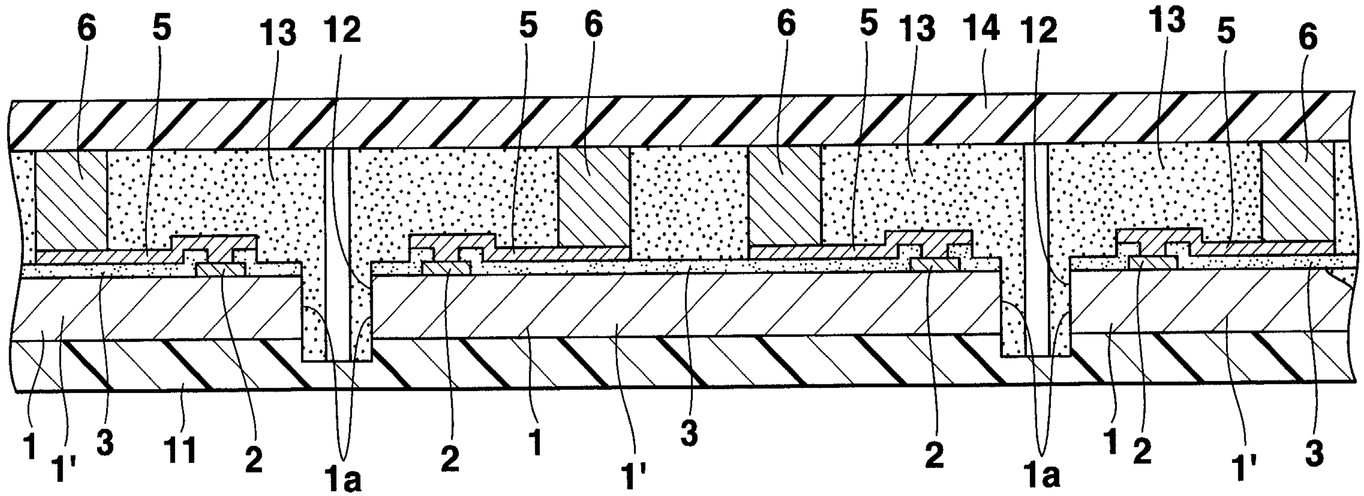


FIG.8

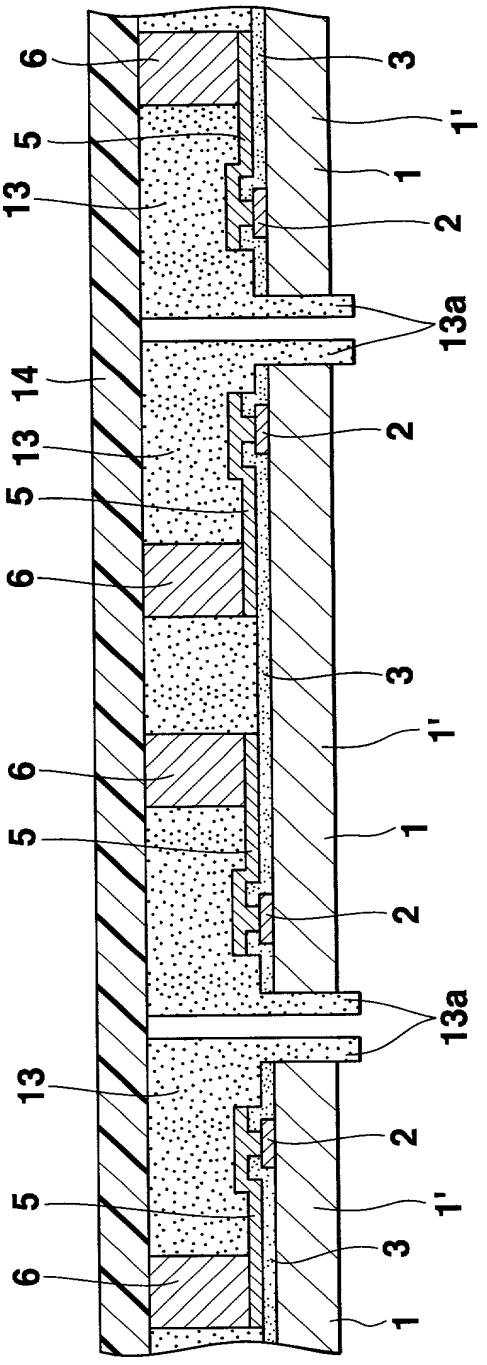


FIG.9

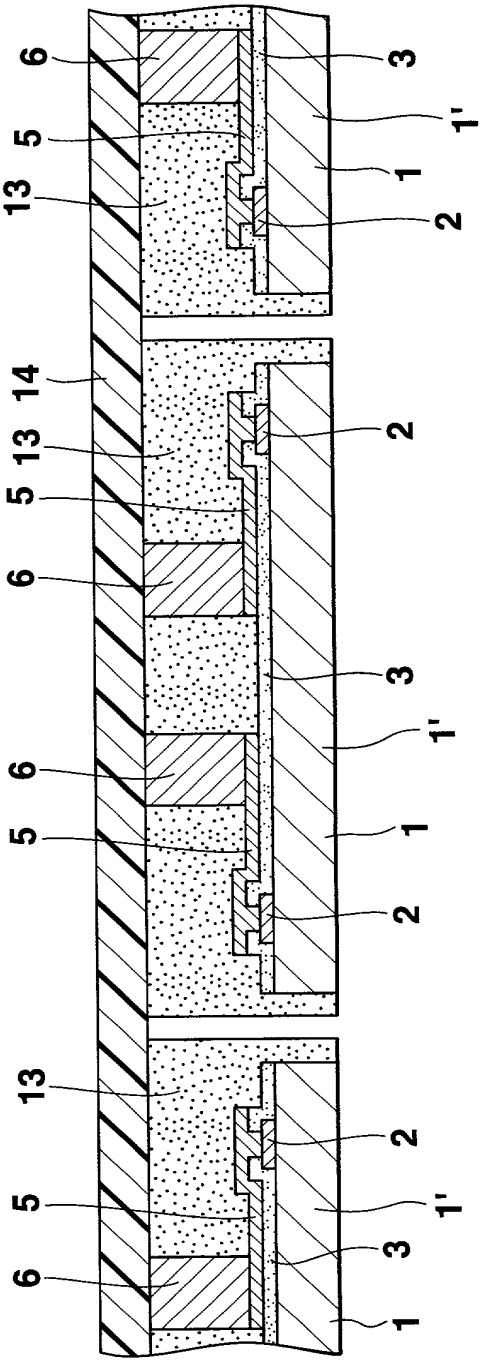


FIG.10

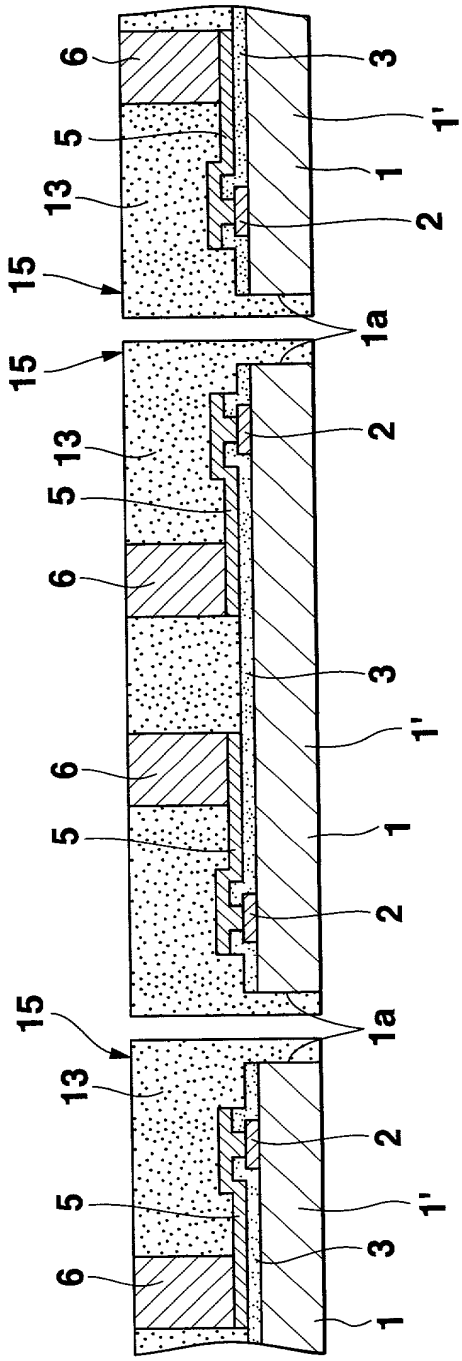


FIG.11

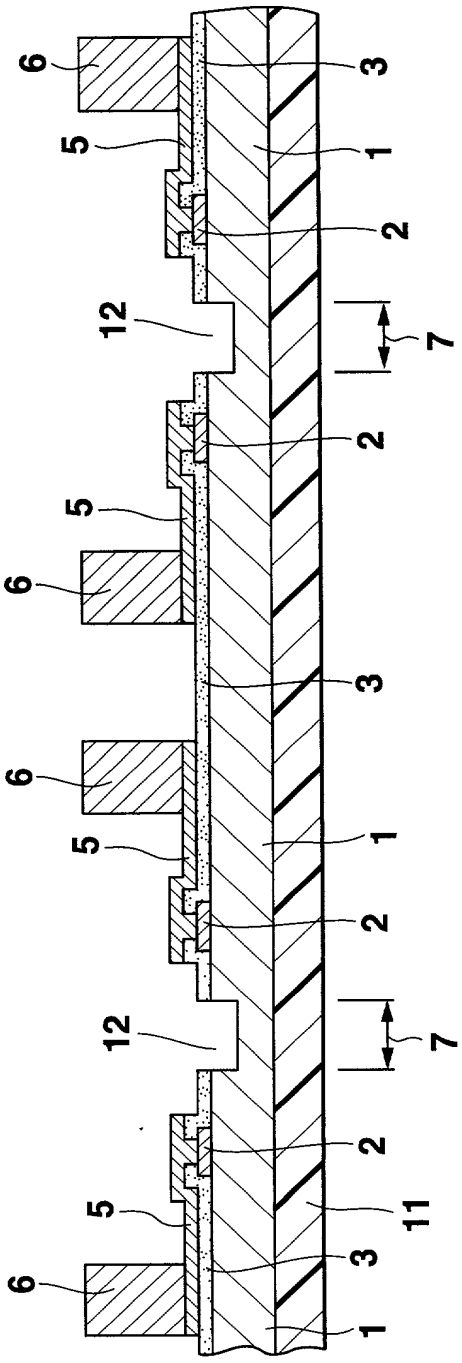


FIG.12

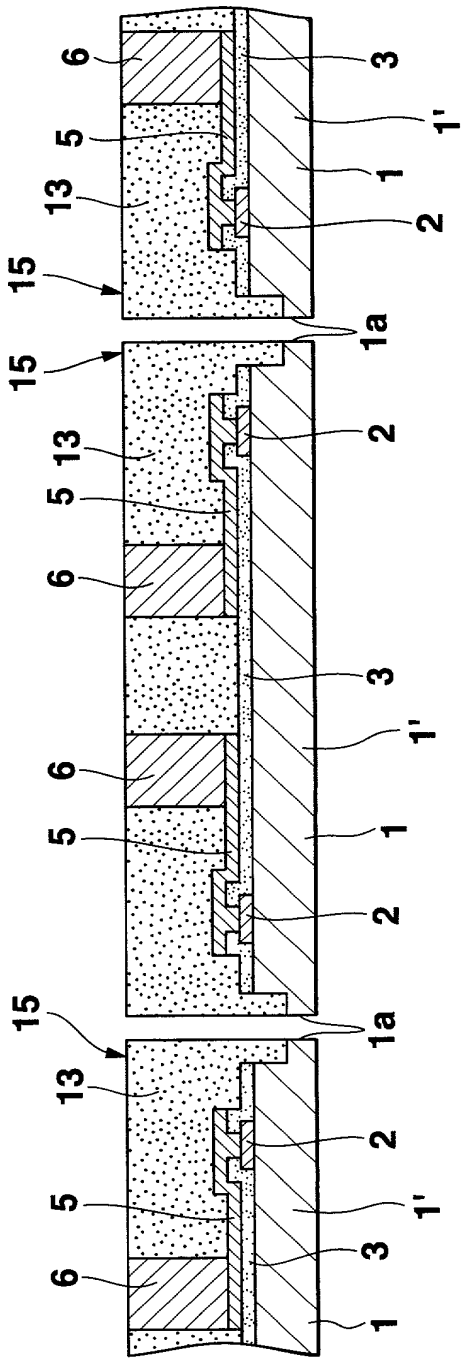


FIG.13

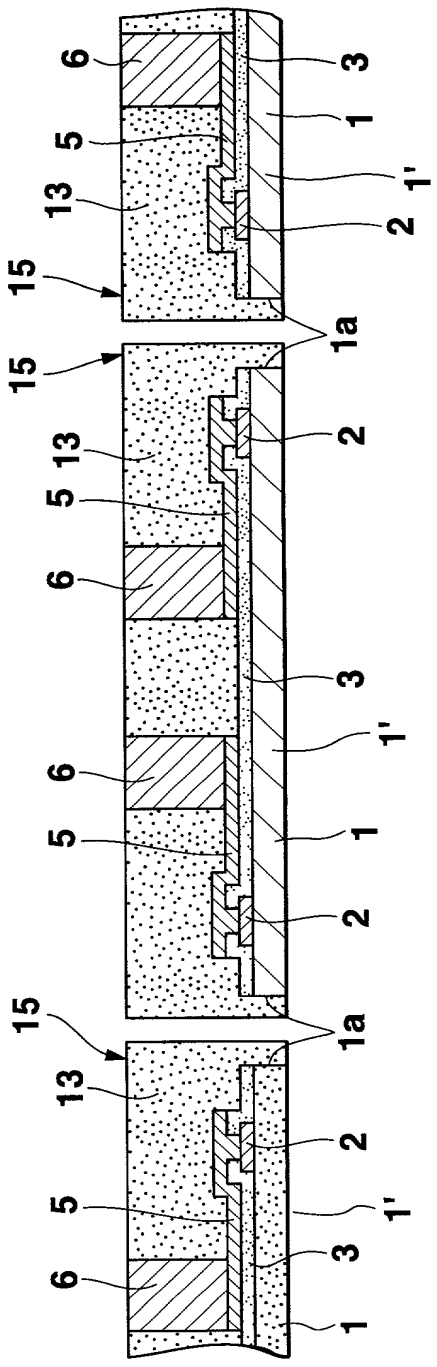


FIG.14

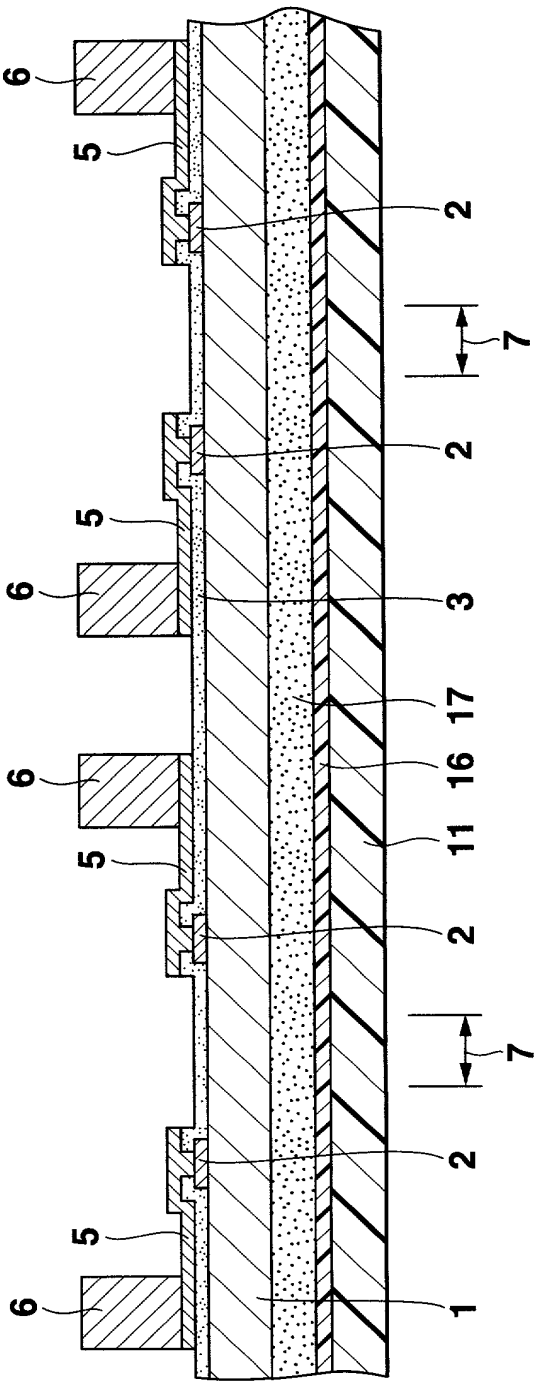


FIG.15

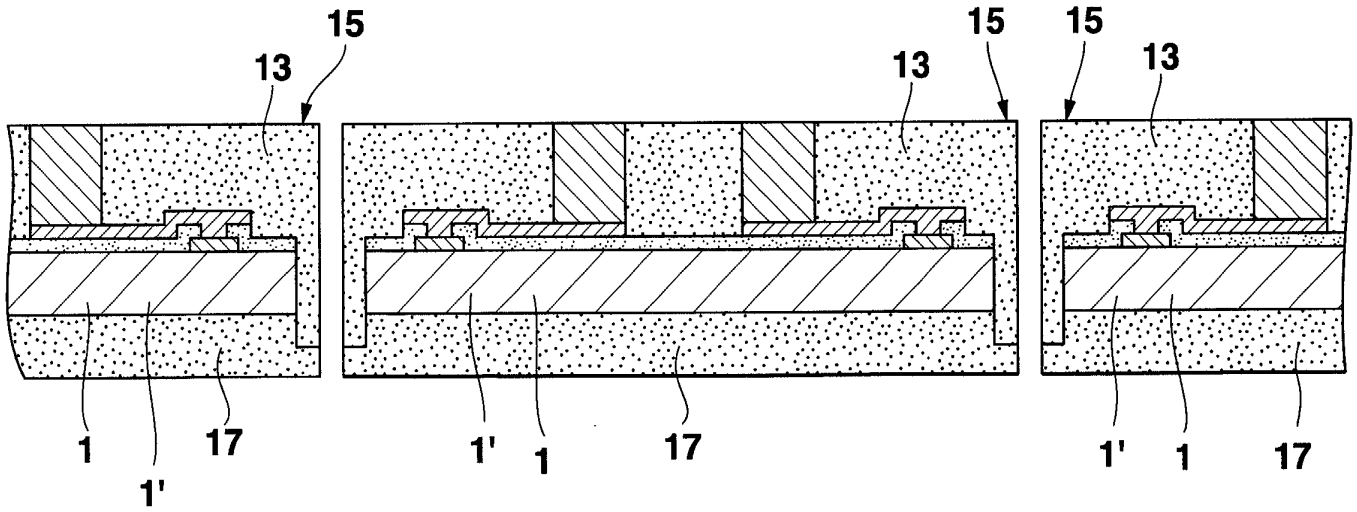


FIG.16

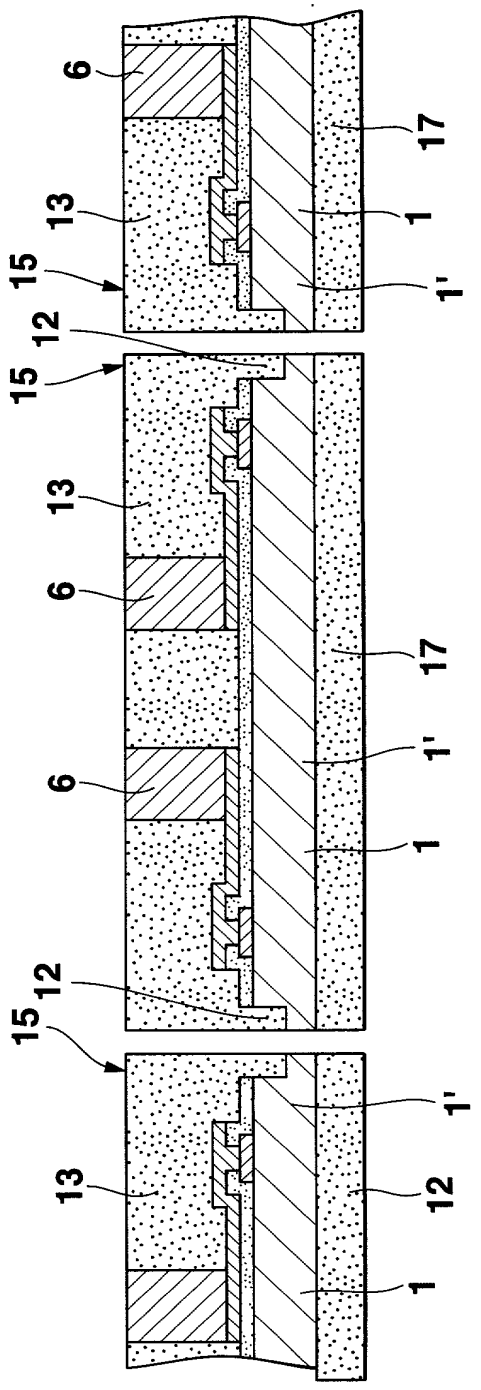


FIG.17
(PRIOR ART)

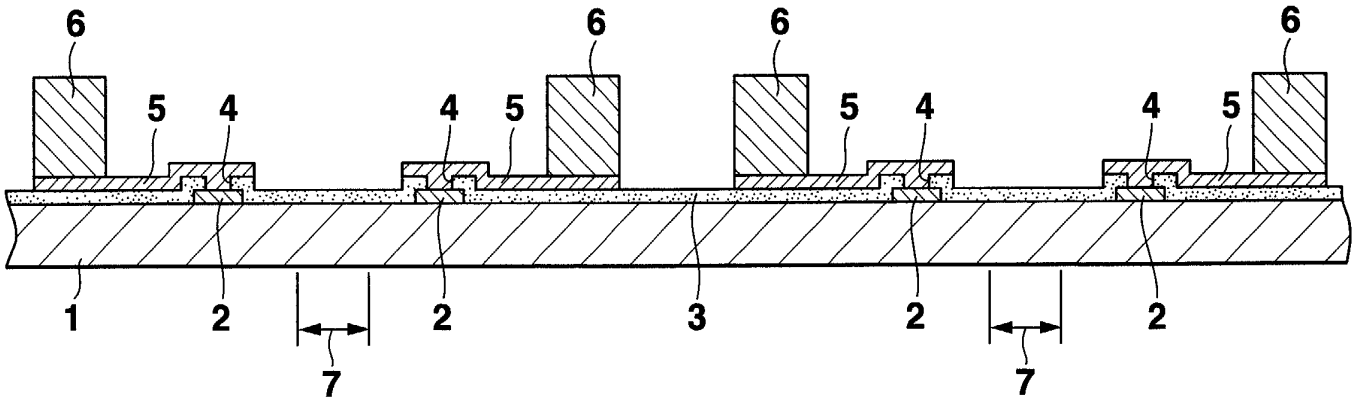


FIG.18
(PRIOR ART)

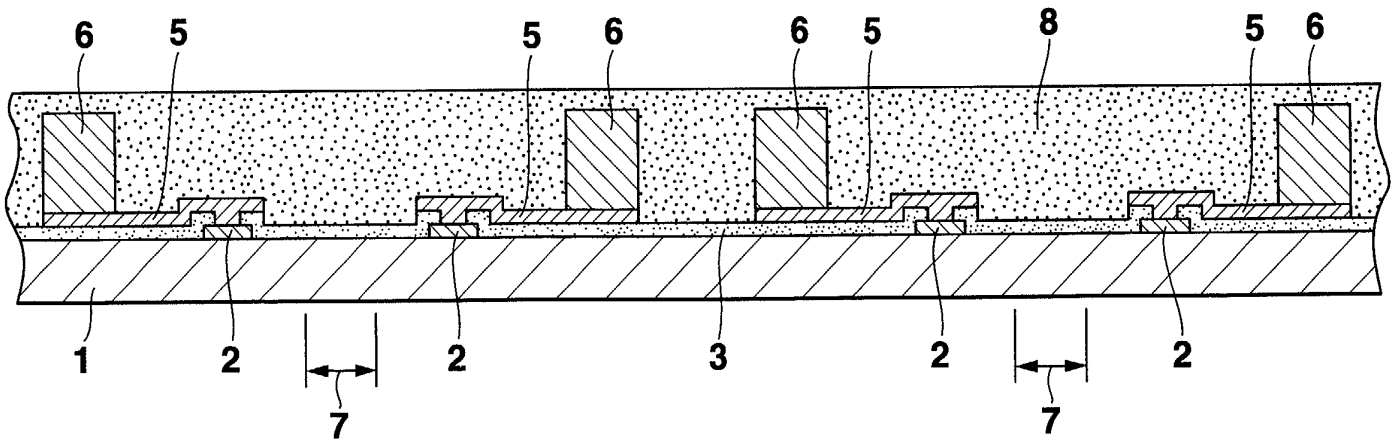


FIG.19
(PRIOR ART)

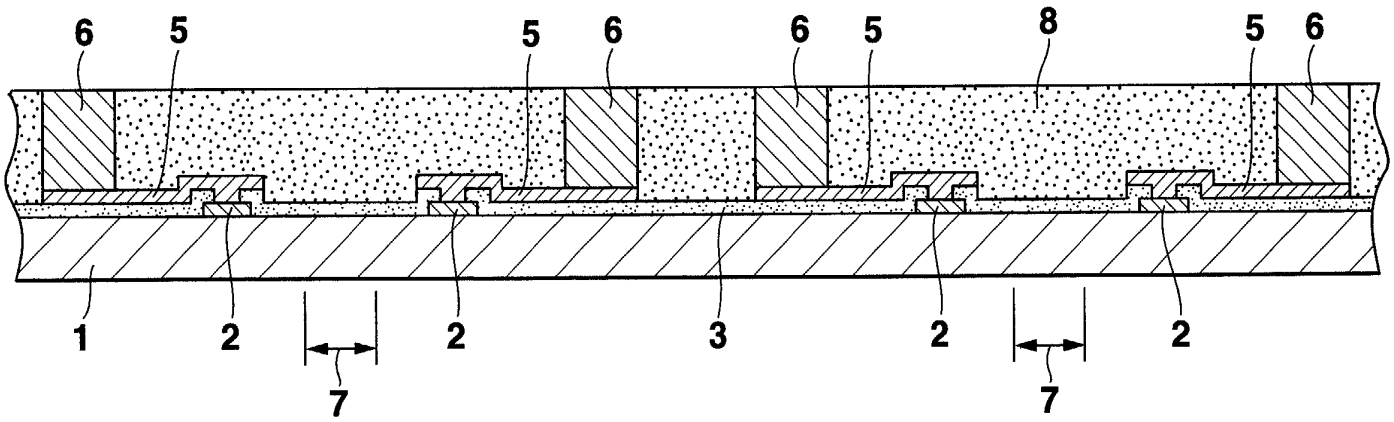
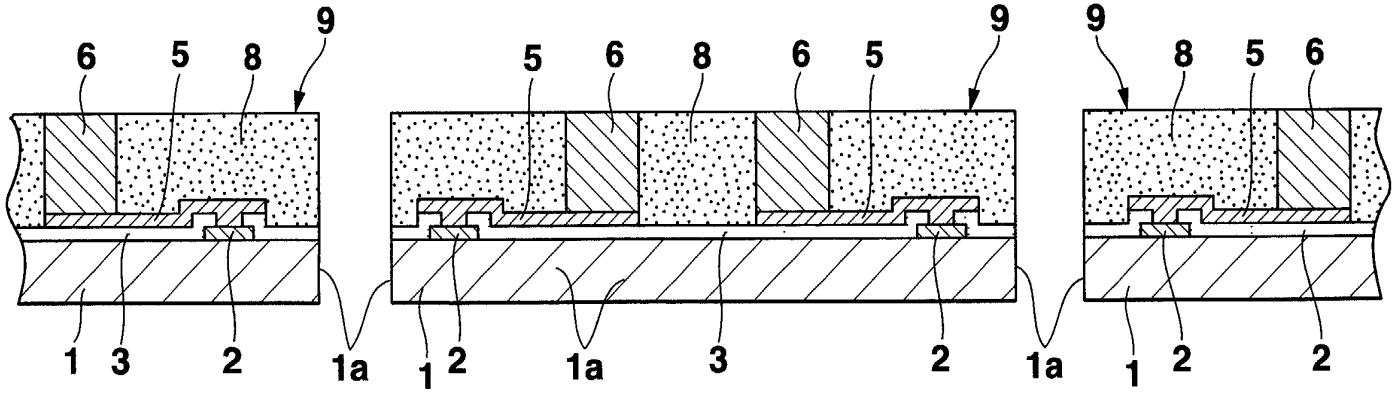


FIG.20
(PRIOR ART)



DECLARATION FOR PATENT APPLICATION

As a below named inventor, I declare:
that I verily believe myself to be the original, first and sole (if only one individual inventor is listed below) or an original, first and joint inventor (if more than one individual inventor is listed below) of the invention in

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

the specification of which is attached hereto unless the following box is checked.

☐ was filed on _____ as United States Application or PCT International Application No._____, and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information of which is material to patentability as defined in 37 CFR 1.56.
I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365 (b) of any foreign application(s) for patent or inventor's certificate, or 35 U.S.C. 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Country	Category	Application No.	Filing Date	Priority Claim
Japan	Patent	11-321416	November 11, 1999	Yes

And I hereby appoint Leonard Holtz (Reg. No. 22,974), Herbert H. Goodman (Reg. No. 17,081), Thomas Langer (Reg. No. 27,264), Marshall J. Chick (Reg. No. 26,853), Richard S. Barth (Reg. No. 28,180), Douglas Holtz (Reg. No. 33,902) and Robert P. Michal (Reg. No. 35,614) each of whose address is 767 Third Avenue - 25th Floor, New York, N.Y. 10017-2023, or any one of them, my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent & Trademark Office connected therewith, and request that correspondence be directed to Frishauf, Holtz, Goodman, Langer & Chick, P.C., 767 Third Avenue - 25th Floor, New York, N.Y. 10017-2023.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

DECLARATION FOR PATENT APPLICATION

I declare further that my citizenship, residence and post office address are as stated below next to my name:

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	Date: Citizen of: Japan	
	Date: Citizen of: Japan	
	Date: Citizen of: Japan	
	Date: Citizen of: Japan	